a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate; and

a semiconductor layer disposed directly on the LTCIM layer.

19. (Added) The SOI structure according to claim 18 further including;

a gate defining a channel interposed between a source and a drain formed within an active region of the SOI structure.

REMARKS

Following entry of this amendment, claims 1-10, and 17-19 will be pending. Claims 11-16 have been canceled. Claims 1 and 17 have been amended. Additionally, claims 18 and 19 have been added.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112

Claims 1-10 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 1 has been amended to correct the antecedent basis pointed out by the Examiner. Specifically, the limitation of "the polysilicon layer" has been amended to read "the LTCIM layer" which has proper antecedent basis. Since claim 1 has proper antecedent basis for the LTCIM layer, the claims 2-10 which depend directly or indirectly from claim 1 also have proper antecedent basis. Therefore, withdrawal of the rejection is respectfully requested for at least the above reason.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 102

Claims 1-10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,773,151 issued to Begley et al.

Begley et al. discloses a bonded wafer which has a silicon device layer bonded to a layer of semi-insulating material. The semi-insulating material is preferably a mobility

degraded silicon, such as polycrystalline silicon. With reference to Figure 8, Begley et al. specifically discloses a bonded wafer, including a handle substrate, preferably of monocrystalline silicon. A semi-insulating layer is disposed over the handle substrate. The semi-insulating layer is preferably silicon in the form of polycrystalline silicon, amorphous silicon, or other forms of silicon including oxygen-doped silicon and porous silicon. The semi-insulating layer is followed by an insulating, silicon dioxide layer which is then bonded to a device layer comprising monocrystalline silicon (col. 1, lines 58-67).

Claim 1 as amended includes the following feature: "a leaking, thermally conductive insulator material (LTCIM) layer disposed **directly** on the semiconductor substrate." Additionally, amended claim 1 includes the following feature "a semiconductor layer disposed **directly** on the LTCIM layer." In other words, the LTCIM layer is interposed between the semiconductor substrate and the semiconductor layer. Examples of support for the LTCIM layer being formed directly on the semiconductor substrate and the semiconductor layer being formed directly on the LTCIM layer are shown in Figure 1, and Figures 3A-3C and described at page 6, lines 7-10 and page 7, lines 11-13.

Begley et al. do not teach or suggest an LTCIM layer that is directly disposed on the semiconductor substrate. Additionally, Begley et al. do not teach or suggest the semiconductor layer that is directly disposed on the LTCIM layer. Begley et al. disclose the semi-insulating layer 14 having a silicon dioxide layer 18 formed thereon. Further Begley et al. disclose the silicon dioxide layer 18 is then bonded to the device layer 20 (col. 1, lines 65-66 and col. 3, lines 1-5).

Claims 1-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,637,513 issued to Sugiyama (Sugiyama).

Sugiyama discloses an SOI structure having a single-crystal silicon layer formed on an insulating structure. A resistive silicon layer is formed on a non-device region of the substrate. The resistive silicon layer may be made of polysilicon or single-crystal silicon. Referring to Figures 9A-9D of Sugiyama, Sugiyama specifically discloses a single-crystal silicon substrate 11, a silicon dioxide layer 12 and a n-type single-crystal silicon layer 19 (see for example, col. 9, lines 1-3).

Sugiyama does not teach or suggest a LTCIM layer that is directly disposed on the semiconductor substrate. Additionally, Sugiyama does not teach or suggest a semiconductor layer is directly disposed on the LTCIM as claimed in amended claim 1. Specifically, the electrically resistive single-crystal silicon layer 19 of Sugiyama is located laterally to the impurity doped regions 13a (see for example, col. 9, lines 10-20).

Claims 1-10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JP7-86298 by Takenori.

Takenori discloses an oxide layer or film formed on a silicon substrate, and an N+ type silicon film 6 formed on the oxide film 20 (see col. 6, lines 32 through col. 7, line 1).

Takenori does not teach or suggest a LTCIM layer disposed directly on a semiconductor substrate nor does Takenori teach or disclose the semiconductor layer disposed directly on the LTCIM layer as described above.

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,569,620 issued to Linn et al.

Linn et al. discloses an SOI wafer. The SOI wafer provides dielectric isolation with silicon dioxide, diamond, silicon-nitride, and so forth. In one embodiment, the bonding silicides provide a thermal dissipating layer between a buried diamond layer and a handle wafer (see for example, Abstract). Referring to Figure 6, Linn et al. discloses a wafer 602 with a diamond film 613 grown thereon and a polysilicon layer 602 deposited on the diamond film 613. Additionally, platinum is deposited on the polysilicon layer 602. The handler wafer silicon reacts with the platinum to form platinum silicide (PtSi) 615 to bind the wafers (see for example, col. 7, lines 36-42). Linn et al. do not teach or suggest an LTCIM layer disposed directly on a semiconductor substrate as claimed in amended claim 1. Additionally, Linn et al. do not teach or suggest a semiconductor layer disposed directly on the LTCIM layer also claimed in amended claim 1.

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,777,365 issued to Yamaguchi et al. (hereinafter Yamaguchi et al.).

Yamaguchi et al. disclose an SOI structure including a buried silicon oxide film 2 with a polycrystalline silicon. The buried silicon oxide film 2 has a thin region 15 below the P-

well region 9. Below the thin region 15 of buried silicon oxide film 2 is a polycrystalline silicon 16 (see for example, col. 4, lines 1-17). Yamaguchi et al. do not teach or suggest a semiconductor layer disposed directly on the LTCIM layer as claimed in amended claim 1.

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,561,303 issued to Schrantz et al. (hereinafter Schrantz et al.).

Schrantz et al. disclose a semiconductor structure comprising a first layer of crystalline material with a layer comprising polycrystalline diamond formed over the first layer. A layer of polycrystalline silicon is formed over the diamond containing layer and a layer of monocrystalline material is formed over the polycrystalline silicon (see, for example, the Abstract). Referring to Figure 5 of Schrantz et al., Schrantz et al. disclose a N- collector region 38 formed in the monocrystalline upper portion 36 and a buried N+ region 40 formed in the polycrystalline silicon lower portion 34. The buried N+ region 40 is formed on the diamond insulator layer 12.

Schrantz et al. do not teach or suggest a LTCIM layer disposed directly on a semiconductor substrate nor do Schrantz et al. teach or suggest the semiconductor layer is directly disposed on the LTCIM layer as claimed in amended claim 1.

Claim 17 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Linn et al. and alternatively as being anticipated by Schrantz et al. Claim 17 has been amended to contain the limitations of a LTCIM layer being disposed directly on a semiconductor substrate and a semiconductor layer disposed directly on the LTCIM layer. For the reasons described above with reference to claim 1, Linn et al. and Schrantz et al. do not teach or suggest a LTCIM layer as claimed in amended claim 17.

Since claims 1 and 17 include one or more limitations not taught or at least suggested by Linn et al., Begley et al., Sugiyama, Takenori, Schrantz et al., or Yamaguchi et al., claims 1 and 17 and those claims that depend directly or indirectly from claim 1 are patentable over Linn et al., Begley et al., Sugiyama, Takenori, Schrantz et al., or Yamaguchi et al. for at least the reasons stated above. Accordingly, reconsideration and withdraw of the rejections under 35 U.S.C. § 102(b) is requested.

NEW CLAIMS

Newly added claims 18 and 19 recite a SOI structure including the limitations of a LTCIM layer "disposed directly on the semiconductor substrate" and "a semiconductor layer disposed directly on the LTCIM layer." As described above, none of the cited art teaches or suggests a LTCIM layer interposed between the semiconductor substrate and the semiconductor layer wherein the LTCIM layer is disposed directly on the semiconductor layer and the semiconductor layer is disposed directly on the LTCIM layer. Therefore, claims 18 and 19 are patentable over Linn et al. Begley et al., Sugiama, Takenori, Schrantz et al., and Yamaguchi et al. alone or in combination.

CONCLUSION

In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present invention.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0988; Our Order No. F0522 (AMDSP0414US).

Respectfully submitted,

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APPENDIX A to

REPLY TO OFFICE ACTION DATED APRIL 10, 2002

In re patent application of:

Applicant: Dong-Hyuk Ju et al.

Serial No: 09/879,724

Filing Date: June 12, 2001

Art Unit: 2826

Examiner: Ahmed N. Sefer

Title: **LEAKY, THERMALLY CONDUCTIVE INSULATOR MATERIAL (LTCIM) IN SEMICONDUCTOR-ON-INSULATOR (SOI) STRUCTURE**

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1. (Amended) A semiconductor-on-insulator (SOI) structure having;

a semiconductor substrate;

a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate; and

a semiconductor layer disposed directly on the LTCIM layer; and

active regions defined in the semiconductor layer by isolation trenches and the LTCIM [~~polysilicon~~] layer.

17. (Amended) A semiconductor-on-insulator (SOI) structure having;

a semiconductor substrate;

a leaky, thermally conductive material (LTCIM) layer disposed directly on the semiconductor substrate;

a semiconductor layer disposed directly on the (LTCIM) layer;

a gate defining a channel interposed between a source and a drain formed within an active region of the SOI structure; and

the active region defined in the semiconductor layer by isolation trenches and the LTCIM layer.